

Applicant respectfully submits that the Examiner has cited no portion of Huckels that describes a "semiconductor device having a DRAM including a cell capacitor formed in a DRAM region of a semiconductor substrate, and a capacitor element formed in an analog element region of the semiconductor substrate" as recited in claim 1. The Examiner stated at page 2 of the Office Action that "Huckels teaches a method comprising: a) simultaneously forming a storage node of the capacitor and lower electrode of the capacitor (Fig. 1 (161) and Col. 2, lines: 34-40) . . ." Huckels as cited by the Examiner, including Fig. 1 element 161 and col. 2, lines 34-40, appears to relate to one trench capacitor formed in a DRAM cell. The Examiner has cited no portion of Huckels describing a "lower electrode of the capacitor" as recited in claim 1.

The Examiner, in responding to applicant's previous response, stated that applicant did not "refer back" to the preamble of the claim. Applicant does not agree with the Examiner's statements regarding the legal standards relating to the preamble and patentability. Moreover, applicant respectfully submits that the language of claim 1 does refer back to the preamble of the claim. The preamble of claim 1 recites in part "a DRAM including a cell capacitor formed in a DRAM region" and "a capacitor element formed in an analog element region". Claim 1, after the preamble, recites in part "simultaneously forming a storage node of the cell capacitor and a lower electrode of the capacitor element . . ." This claim element refers to "a storage node of the cell capacitor" and to "a lower electrode of the capacitor element". These underlined terms clearly refer back to the preamble and indicate that the "cell capacitor" is "formed in a DRAM region" and the "capacitor element" is formed "in an analog element region". As the Examiner has cited no portion of the art describing or suggesting "simultaneously forming a storage node of the cell capacitor and a lower electrode of the capacitor element" as recited in claim 1, the rejection should be withdrawn for at least this reason. Applicant also respectfully submits that the other elements of claim 1 are not described or suggested by the Examiner's citations to Huckels.

Claims 2-8 depend from claim 1 and the rejection of these claims should be withdrawn for at least the same reasons as for claim 1. In addition to the reasons explained above for claim 1, applicant respectfully submits that the Examiner's citations to Huckels do not describe or suggests the elements of claims 2-8.

The Examiner's rejection of claim 15 and its dependent claims 16-23 are deficient for at least similar reasons as claim 1 as explained above and should be withdrawn for at least the same reasons as for claim 1. In addition, applicant respectfully submits that the Examiner's citations to Huckels do not describe or suggests the elements of claims 16-23.

Applicant has added new claim 24. It is believed that no new matter has been entered. Support for claim 24 may be found throughout the specification and in the original claims. Examination of the new claim is respectfully requested.

Applicant further notes that it appears that the Examiner did not initial the pending U.S. patent applications cited on for PTO-1449 submitted by applicant. Applicant submitted copies of these applications with the other IDS papers and does not understand why they were not initialed.

Attached hereto is a marked-up version of the claim changes made by the present amendment. The attached page is captioned "Version with markings to show changes made."

Applicant respectfully submits that claims 1-8 and 15-24 are in condition for allowance. Reexamination and reconsideration are respectfully requested. If, for any reason, the application is not in condition for allowance, the Examiner requested to telephone the undersigned to discuss the steps necessary to place the application into condition for allowance.

Respectfully submitted,

Alan S. Raynes

Reg. No. 39,809

KONRAD RAYNES VICTOR & MANN, LLP

315 South Beverly Drive, Suite 210

Beverly Hills, CA 90212

Customer No. 24033

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(310) 556-7983 (tele general)

(310) 871-8448 (tele direct)

(310) 556-7984 (facsimile)

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Alan S. Raynes

March 3, 2003
(Date)

Version With Markings to Show Changes Made

Claim 16 has been amended as follows:

16. (twice amended) A method according to claim 15, further comprising, prior to forming the storage node of the cell capacitor and the lower electrode of the capacitor element, forming an additional conducting [conducting] layer and etching the additional conducting layer to form a word line that is a component of the DRAM and to form a connection layer that is located in a common layer of the word line and that is configured to electrically connect the lower electrode to another element in the semiconductor device.